IN THE CLAIMS:

Please cancel claims 1-14 and 20-24 without prejudice or disclaimer and amend the remaining claims as follows:

1-14. (canceled).

15. (currently amended) A liquid crystal on silicon imaging device, comprising:

a cover glass;

a silicon backplane physically connected to the cover glass in a connection area; and

a liquid crystal sealed between said cover glass and said silicon backplane;

wherein said silicon backplane comprises:

a frame buffer configured to store pixel data;

a pixel array;

an interface control block connected between the frame buffer and the pixel array, the interface control block being adapted to determine pulse width modulation waveforms for the pixel array in accordance with the pixel data stored in the frame buffer; ~~and~~

an external interface block configured to provide an external interface to the device, including receiving pixel data and transferring the received pixel data into the frame buffer; and

a control block connected to the external interface block, the frame buffer, and the interface control block, the control circuit being adapted to provide control signals to operate the device.

16. (original) The liquid crystal on silicon imaging device as recited in claim 15, wherein at least a portion of the frame buffer block includes memory cells co-located with pixel elements of the pixel array.

17. (original) The liquid crystal on silicon imaging device as recited in claim 15, wherein the frame buffer includes a front buffer and a back buffer.

18. (original) The liquid crystal on silicon imaging device as recited in claim 15, wherein the frame buffer, the interface control block and the control block are located on a periphery of the device and at least partially fit within the connection area where the cover glass is attached to the backplane.

19. (original) The liquid crystal on silicon imaging device as recited in claim 18, wherein the frame buffer, the interface control block, and the pixel array are divided into first and second parts, wherein the first part is associated with a first half of rows of the pixel array and the second part is associated with a second half of rows of the pixel array.

20-24. (canceled).

Please add the following new claims:

25. (Newly added) A display system, comprising:

a light engine;

a projection lens; and

a liquid crystal on silicon imaging device, comprising:

a cover glass;

a silicon backplane physically connected to the cover glass in a connection area; and

a liquid crystal sealed between said cover glass and said silicon backplane;

wherein said silicon backplane comprises:

a frame buffer configured to store pixel data;

a pixel array;

an interface control block connected between the frame buffer and the pixel array, the interface control block being adapted to determine pulse width modulation waveforms for the pixel array in accordance with the pixel data stored in the frame buffer;

an external interface block configured to provide an external interface to the device, including receiving pixel data and transferring the received pixel data into the frame buffer; and

a control block connected to the external interface block, the frame buffer, and the interface control block, the control circuit being adapted to provide control signals to operate the device.

26. (Newly added) The display system as recited in claim 25, wherein at least a portion of the frame buffer block includes memory cells co-located with pixel elements of the pixel array.

27. (Newly added) The display system as recited in claim 25, wherein the frame buffer includes a front buffer and a back buffer.

28. (Newly added) The display system as recited in claim 25, wherein the frame buffer, the interface control block and the control block are located on a periphery of the device and at least partially fit within the connection area where the cover glass is attached to the backplane.

29. (Newly added) The display system as recited in claim 28, wherein the frame buffer, the interface control block, and the pixel array are divided into first and second parts, wherein the first part is associated with a first half of rows of the pixel array and the second part is associated with a second half of rows of the pixel array.

30. (Newly added) A method, comprising:

providing a single silicon backplane;

providing a frame buffer on the silicon backplane;

providing a pixel array on the silicon backplane;

providing an interface control block connected between the frame buffer and the pixel array on the silicon backplane, the interface control block being adapted to determine pulse width modulation waveforms for the pixel array in accordance with the pixel data stored in the frame buffer;

providing an external interface block on the silicon backplane, the external interface block being configured to provide an external interface, including receiving pixel data and transferring the received pixel data into the frame buffer; and

providing a control block on the silicon backplane, the control block being connected to the external interface block, the frame buffer, and the interface control block, the control circuit being adapted to provide control signals.

31. (Newly added) The method as recited in claim 30, further comprising:

co-locating at least a portion of the frame buffer block with pixel elements of the pixel array.

32. (Newly added) The method as recited in claim 30, wherein the frame buffer includes a front buffer and a back buffer.

33. (Newly added) The method as recited in claim 30, further comprising:

locating the frame buffer, the interface control block and the control block on a periphery of the silicon backplane and at least partially within a connection area where a cover glass is to be attached to the backplane.

34. (Newly added) The method as recited in claim 33, wherein the frame buffer, the interface control block, and the pixel array are divided into first and second parts, wherein the first part is associated with a first half of rows of the pixel array and the second part is associated with a second half of rows of the pixel array.